CLAIMS:

1. A backplane comprising an array of electrical or electronic elements and at least one separate spacer which rises higher over the backplane than said array, and comprises at least two layers essentially of the same material and occurring in the same order as is found in at least one of the electrical or electronic elements.

2. A backplane according to claim 1 wherein the backplane is a semiconductor backplane.

Sub. A1

3. A backplane according to claim 1 or claim 2 wherein the spacer comprises a series of more than two said layers.

4. A backplane according to any preceding claim wherein at least one of said two layers is modified in one of said spacer and said electrical or electronic element relative to the other of said spacer and said electrical or electronic element.

5. A backplane according to any preceding claim wherein all the layers in the spacer correspond in material and order to those found in the said at least one electrical or electronic element.

6. A backplane according to any preceding claim wherein the spacer is overall electrically insulating between top and bottom.

7. A backplane according to any preceding claim wherein there is a plurality of said spacers distributed over the backplane.

8. A backplane according to claim 7 wherein at least some of the spacers are regularly distributed over the array.

Sub. A2

9. A backplane according to claim 7 or claim 8 wherein the array provides a plurality of addressable locations, and each location has at least one said spacer associated therewith.

10. A backplane according to claim 9 wherein each location has only one said spacer associated therewith

Sub. A3

11. A backplane according to any one of claims 7 to 10 wherein at least one said spacer is in the form of a column having a generally square cross-section.

12. A backplane according to any one of claims 7 to 11 wherein at least one said spacer is in the form of a ridge having an elongate cross-section.

13. A backplane according to any preceding claim wherein said array is covered by an insulating layer which also extends over the said spacer or said plurality of spacers.

14. A backplane according to claim 13 wherein said insulating layer has a generally constant thickness.

15. A backplane according to claim 13 wherein the upper surface of said insulating layer is substantially flat.

Sub. A4

16. A backplane according to any one of claims 13 to 15 wherein an electrode is deposited on said insulating layer and is coupled to a said element of said array.

17. A backplane according to claim 16 wherein said electrode is reflective.

18. A backplane according to claim 17 wherein the reflectivity of the electrode is greater than the reflectivity of conductive layers occurring in the electrical or electronic element and/or spacers of the array.

Sub. A5

19. A backplane according to any preceding claim wherein the top surface thereof is treated in a manner to induce liquid crystal alignment.

20. A backplane according to any preceding claim wherein the backplane is an active backplane in which the array comprises active electronic elements.

Sub AS concluded

21. A backplane according to any preceding claim wherein at least some of the spacers are located externally of the array.

22. A backplane according to any preceding claim wherein the array is connected to other circuitry formed on the backplane but spaced from the array by a lane.

23 A backplane according to claim 21 and claim 22 wherein said externally located spacers are located in said lane.

24. A backplane according to claim 22 or claim 23 wherein the said lane is of sufficient width to permit the presence of an adhesive sealing strip without substantial contact with the array and said other circuitry.

25. A backplane according to any one of claims 22 to 24 wherein the width of the lane is least 500 microns.

26. A backplane according to claim 25 wherein the width of the lane is least 1500 microns.

Sub AS

27. A backplane according to any one of claims 22 to 26 wherein the said circuitry connected to the array comprises logic for addressing elements of the array.

28. A method of producing a backplane as defined in any preceding claim, wherein processes used for making parts of at least one said element are also used simultaneously to form parts of said spacers.

29. A method of producing a backplane having at least one region containing an array of electrical or electronic elements, wherein the processes used for making parts of at least one said element are also used simultaneously to form parts of spacers on the backplane laterally spaced from said elements.

30. A method according to claim 29 wherein said backplane is a semiconductor backplane.

31. A method of producing a backplane according to claim 29 or claim 30 wherein the spacers comprise at least two layers of substantially the same material and occurring in the same order as is found in at least one said electrical or electronic element.

32. A cell comprising a backplane as defined in any one of claims 1 to 26 and an opposed electrode sealed thereto in spaced relation.

33. A cell according to claim 31 wherein liquid crystal material is located between the electrode and the backplane.

34. A cell according to claim 33 wherein the liquid crystal material has a smectic phase.